ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 2, Issue 4, April 2014

Design of High speed, Low Power Pipelined ADC

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Abstract: An 8-bit pipelined analog-to digital converter (ADC) is designed in this paper. The pipelined architecture realizes the high-speed and high-resolution . To reduce some complexities of flash ADC pipeline ADC is used. The calibration schemes of pipelined ADC limit absolute and relative accuracy. Deviations in residue amplifier gain results due to low intrinsic gain of transistors, and mismatching between all the capacitors of capacitance 1pF result in both deviations in residue amplifier gain and DAC nonlinearity in a pipelined ADC.

Keywords: Comparator, Folded Opamp, SUB-ADC,MDAC, Digital Error Correction block(DEC), Time Alignment Block

I. INTRODUCTION

The proposed architecture consists by means of 7 separate 1.5 bit ADC sub-blocks, 1 MDAC block and 1 SHA block with open loop gain of 2. Every block takes equal interval of time to evaluate residue and generate 1.5-bit of digital output. The focus of this paper will be the power reduction techniques on the architectural level, such as the choice of time alignment and digital correction. The key factor of designing the circuit is to ensure that the all the ADC data conversion ends within the scheduled time interval. Output of ADC is 11, 01 or 00 in thermometer code format. To obtain binary output code the thermometer codes converted by the help of encoder into digital outputs bits 10, 01 or 00 respectively. The resolution each stage is chosen at 1.5 bit, mainly because of two main reasons, the tolerance on the comparator offset can be as much as $\pm 0.25 V_{REF}$ and the low closed loop gain for the SC circuit is essential for high speed operation. For the noise requirement the capacitors in each stage is scaled properly.

II. SUB-CIRCUITS OF PIPELINED ADC

The pipelined ADC have the non-ideal factors which includes the switching charge injection, op-amp finite open-loop gain, input parasitic capacitance and thermal noise.Fig.1 shows the complete architectural design of 8 bit pipelined ADC. Input supply voltage of 1volt is supplied to SHA, and that will pass through each sub-converter stage of ADC. This pipeline stage gives rise to 8 bit resolution.SHA is the heart of pipelined ADC. So reduce the power, we have to reduce the power of SHA circuit. If the resolution of ADC increases then automatically power consumption, noise and error will increases[2].

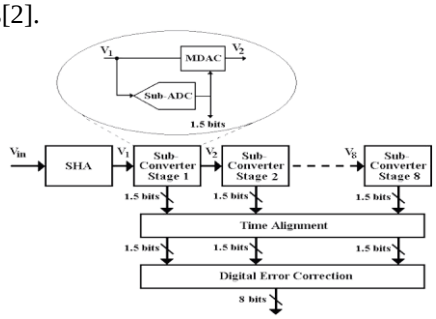

Fig 1.pipelined ADC[1]

III. COMPARATOR

For the pipelined ADCs latched comparator is used. When ϕ_{latch} goes high 1, the gain transistors gets turn on, it amplifies the differential signal at the inputs V_{in} which is further amplified by the positive feedback action of the latch as the comparator goes into latch mode. The latch output is then applied to inverters sized in such a way as to lower the threshold point to prevent errors of comparator [4].Outputs of ADC remains 0 until the comparator has sufficient overdrive voltage to cause one output to toggle high. For resolution lower than 3 bits, dynamic comparators can be used for the inter-stage ADCs since they do not consume dc power. ADC will need to be preceded by continuous time preamplifiers to reduce the switch charge injection on the input signal and reference voltages V_{REF}. Fig 2 shows the schematic of comparator, Fig 3 and fig 4 shows the output and layout of comparator.

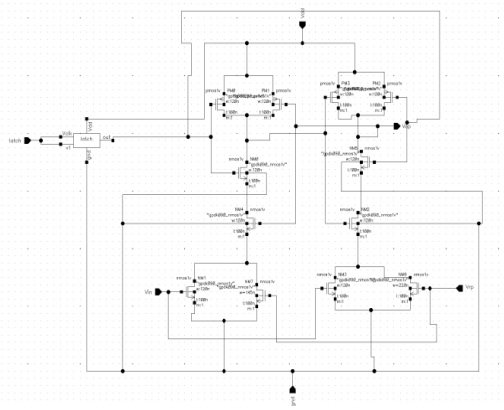

Fig 2.schematic of comparator

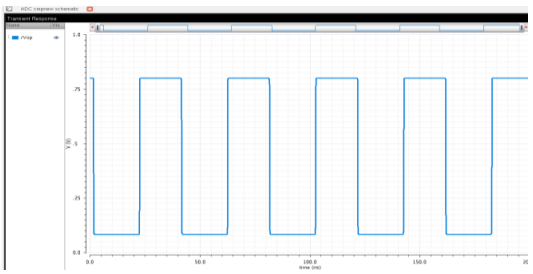

Fig 3.output of comparator

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The design implementation of comparator consists of a latch stage preceded by coupling capacitors that are precharged to the input signal and reference voltages during the reset phase.

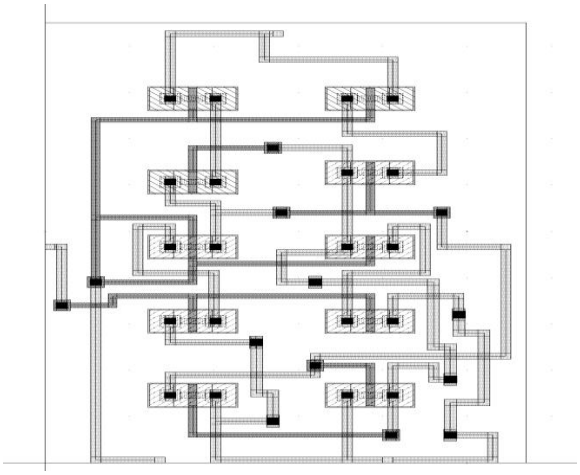

Fig 4. Layout of comparator

25.30microwatt dc power is dissipating in this dynamic comparator with 0.8volt of output voltage.

IV. LATCH

Fig 5 shows the latch circuit which will be further used for latched comparator. Fig 6 and 7 shows the output and layout of latch circuit

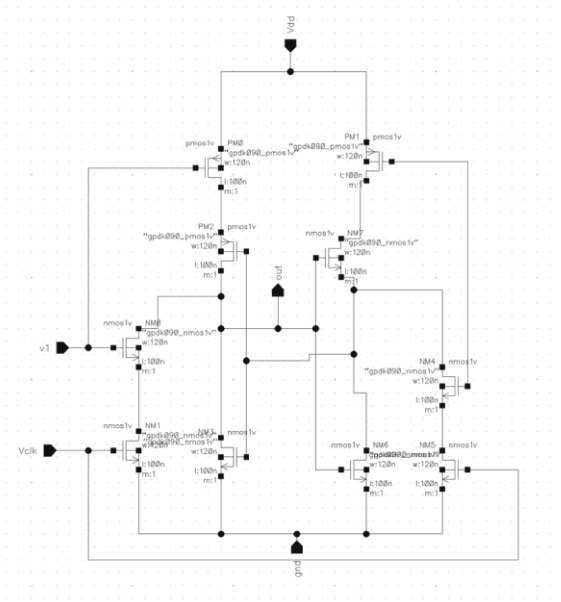

Fig 5.schematic of latch.

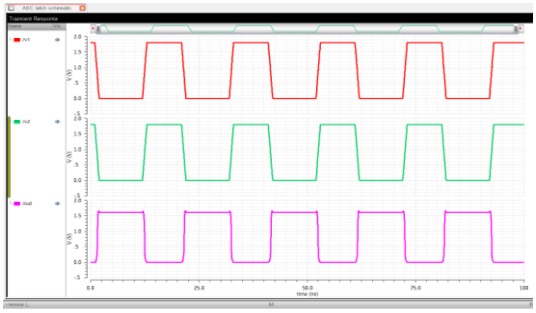

Fig 6.output of latch

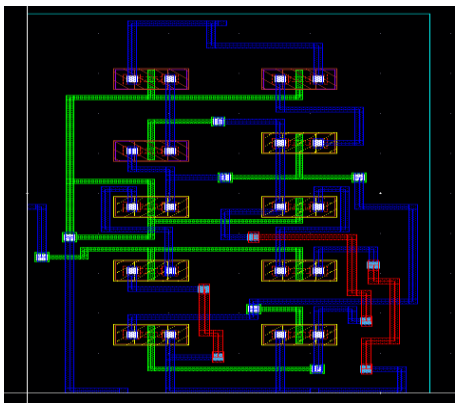

Fig 7. Layout of Latch

V. FOLDED CASCODE OPAMP

For the reduction of power consumption in pipeline ADCs, with proposing the concept of operational amplifier Folded cascade opamp is used for the designing of MDAC and SUB-ADC. Scaling of capacitor done across the pipeline ADC has also been used to decrease power consumption by the capacitor size for each subsequent stages since noise is also going to reduce. Optimization of inter-stage partitioning at lower supply voltage of 1volt with a 8-bit design used as reference.

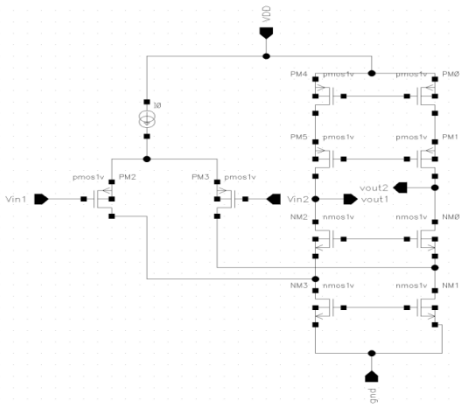

Fig 8.schematic of folded cascade opamp[5]

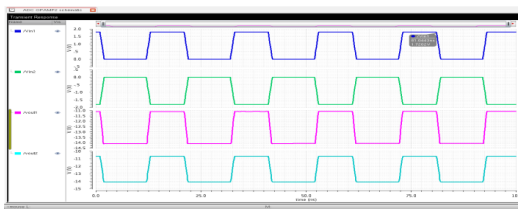

Fig 9.output of folded cascade opamp

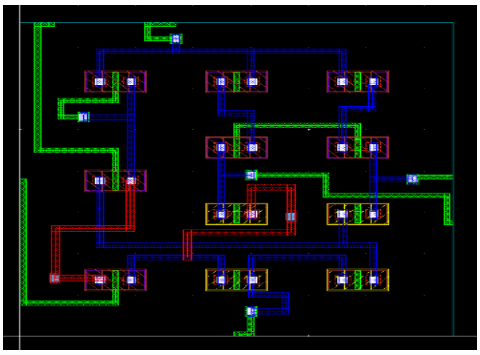

Fig 10. Layout of opamp

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INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
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Fig 8 shows the schematic of folded cascade opamp with its output by fig 9 and complete layout in fig 10.

VI. MDAC

Capacitor-ratioed MDAC(multiplying digital-to-analog converters) commonly used in pipelined ADC's. Digital calibration technique is implemented in MDAC C_{comp} symbol indicates the comparator preamplifier's input capacitance, R_{switch} symbol indicates the first MDAC sampling switch on-resistance, and likewise C_s is the first MDAC sampling capacitor. The bandwidth of the MDAC and the comparator should be slightly higher than or equal as their input time-constants to minimize the noise and errors. Two pairs of nMOS switches are taken for the MDAC; one with input supply voltage of 2V to reduce its on-resistance and the other bootstrapped by superimposing the input voltage at the switch's source terminal on the supply voltage connected to the switch's gate when the switch is on. To realize the SHA it uses a single amplifier and residue amplification. At the first phase (ϕ_1), is sampled onto C_s. The sub-ADC samples the signal at this instance with the DAC providing the quantized value (V_{DAC}) of the input voltage signal. At the second-phase (ϕ_2), the sampled signal is subtracted from the DAC output and held on the amplifier feedback capacitor(C_f). The ratio of C_f to C_s gives the amplifier feedback factor. By holding the amplifier input at the common-mode voltage (V_{CM}) during sampling, the effect of amplifier input parasitic capacitance C_S on is mitigated. Fig 11 shows the schematic of MDAC and fig 12 shows the complete layout.

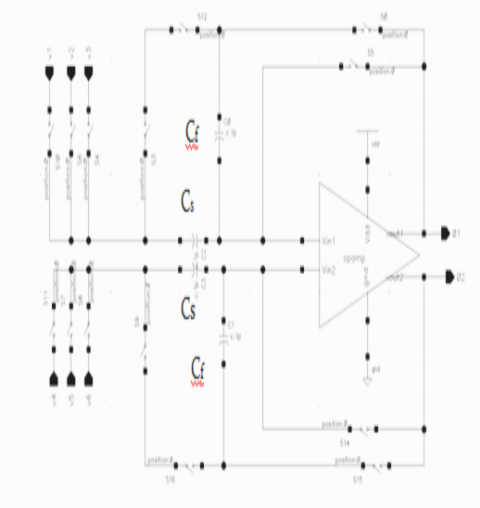

Fig 11. schematic of MDAC[1]

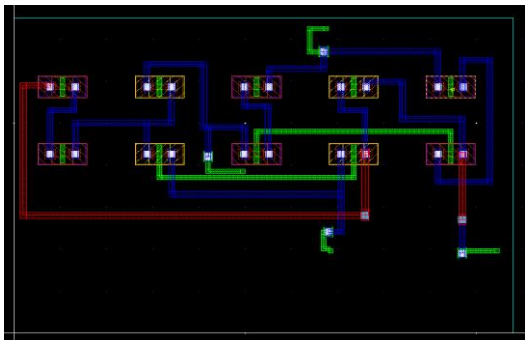

Fig 12. Layout of MDAC

Since the first MDAC's input sampling switches independently sample a time-variant input signal, they need to be highly linear to decrease the signal distortion introduced as a result of sampling. All other switches sample a completely settled time-invariant discrete-time signal and, as such, do not introduce distortion, do not have to be highly linear, and can be made smaller in size than the sampling switches. The MDAC sampling switches are thus reset to linearize them[3]. . At , ϕ_1 the first MDAC samples the input signal onto sampling capacitor Cs with 2 pF capacitance . At the falling edge of the input signal is frozen onto switched capacitor Cs . At the same time, the bottom plate of switched capacitor Cs is connected to the DAC output.

VII. SHA

SHA plays a vital role in designing the ADC. Once the SHA has converted the input analog signal to the digital time signal, the pipeline can now quantize the held signal accurately without subsidize signal-dependent noise. The drawback of SHA is a momentous increase in power consumption for the whole ADC. Subsequently if SHA block is removed, leading to aperture error the relative uncertainty between sub-ADC and MDAC input signal sampling points that need to be allocated by the matching of the first-stage MDAC and sub-ADC comparator sampling networks in terms of time-constants.

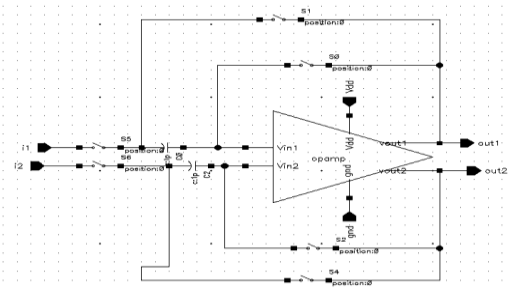

Fig 13. schematic of SHA

VIII. SUB-ADC

The most analytical block of a pipeline ADC is the multiplying D/A converter (MDAC), which performs the D/A conversion of the sub-ADC output, subtraction of the resulting analog signal from the sampled and hold input signal, and amplification of the residue. An MDAC is implemented using the switched capacitor technique, the core of the MDAC being essentially an SC integrator formed around an operational amplifier opamp. The sub-ADC comparator outputs are sustained and used to switch out the correct ladder voltage onto the DAC output nodes. Fig 14 is showing the schematic of sub-ADC. MDAC with SUB-ADC block is shown in the figure 15.

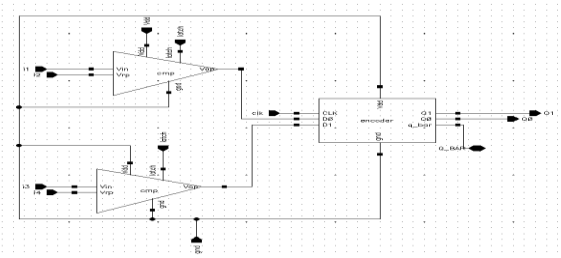

Fig 14.schematic of SUB-ADC

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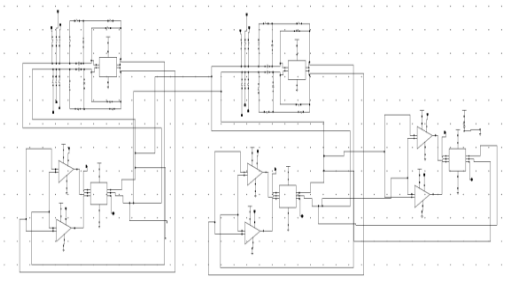

Fig 15. MDAC with SUB-ADC

IX. DIGITAL ERROR CORRECTION CIRCUIT

The digital error correction block is the series of full adders, ensure that the digital output of pipelined ADC does not get affected due to presence of offsets in the comparators of the 1.5 bit ADC sub-block. Two half adders are connected at the both end of series full adders. Error correction is proficient with 1.5-bit ADC and adder blocks. [a0-a7] and [b0-b7] are input bits of ADC ; they are given as input to adder stack as shown.[c0- c7] represents carry. Final digital corrected output is the total sums [s0-s7] . When an offset develops in the sub-ADC ,the output of the first stage will overtake the range defined by $\pm V_{REF}$. when a sub-ADC error is present without digital correction, the error will occur in the digital output. If digital correction block is not used, then the first stage sub-ADC will stay in linear as the entire converter. Whereas in later stages, because of inter stage gain, the requirements can be overcome . If the first stage is ideal, the a full scale input to the first stage, the output is only between -0.5 V_{REF} and +0.5 V_{REF} , leaving an extra bit on the bottom of the per-stage resolution. Digital correction employs the extra bit to correct the overranging section from the previous stage. Fig 16 shows the schematic of digital error correction block, and its output is shown by fig 17.

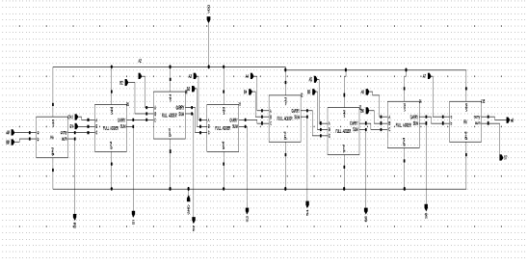

Fig 16. Schematic of digital error correction block

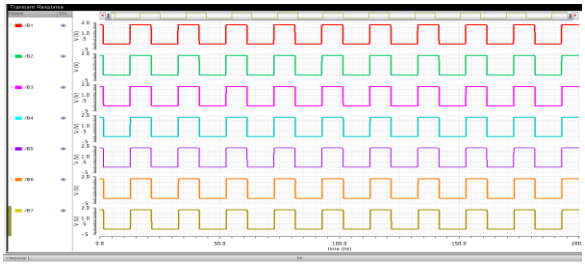

Fig 17. output of Digital Error Correction Block

X. TIME ALIGNMENT BLOCK

Instead of series of buffer shift register block is used to reduce the delay. Shift register block is only a series of D f/f, means output of 1st D f/f is connected with 2nd one. For n bit pipelined ADC n-1 number of shift registers are needed. Digital approximation is the combine factor of sub-ADC and MDAC with processing rate of 1sample per cycle. SHA allows the DAPRX to immediately used to process the next input signal before succeeding DAPRX has finished as long as the preceding DAPRX's digital output is also stored.

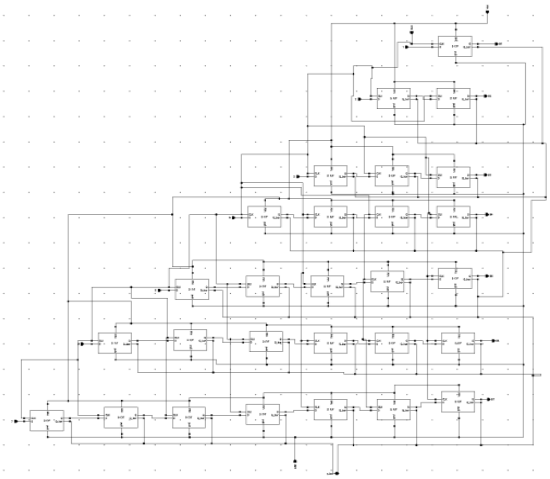

Fig 18. Schematic of Time alignment block

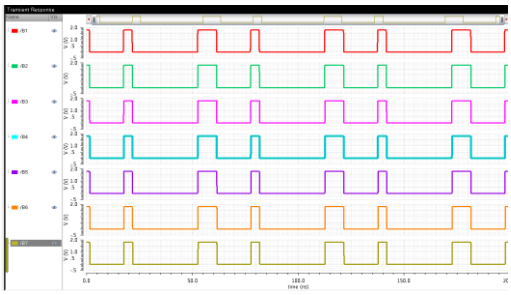

Fig 19. output of Time alignment block

XI. COMPLETE PIPELINED ADC ARCHITECTURE

The analog signal is first sampled by sample and hold amplifier and then quantized by the 1.5 bit ADC in the first stage. The D/A, subtraction and amplification are proficient by the switching capacitor circuit. The amplified output is then sampled by the second stage and then identical operations are performed. The stages are interleaving and hence, the data is handled jointly. Therefore, high throughput can be achieved with this pipelined architecture. The output in form of digital bits from each stage are then collected and digitally corrected by digital error correction block to achieve the 8 bit resolution. Table 1 shows the design and specifications of 8 bit pipelined ADC.

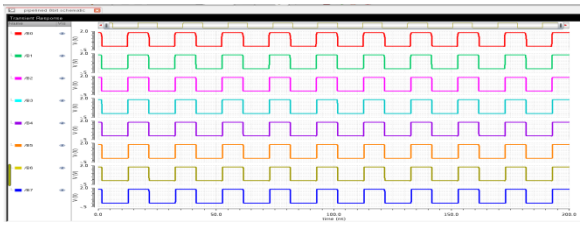

Fig 21. output of Pipelined ADC

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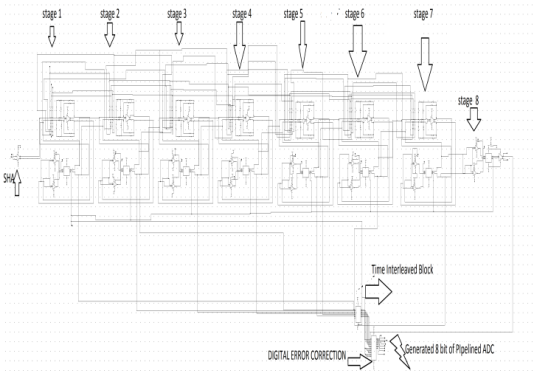

Fig 20. schematic of pipelined ADC

TABLE-1

Design	Specification
Technology	90nm
Input capacitance	1pf
Supply voltage	1 Volt
Reference voltage	0.5Volt
V_{LSB}	0.001
Average power consumption	1.92mW
Peak power	0.53nW
ENOB	7.94bits
Designed ADC resolution	8bits
$(SNR)_{max}$ $(SNR)_{actual}$	49.920db 49.7db
THD	60.429db
SFDR	65db
SINAD	49.55db
SNDR	49.5db
Active area	104.6micrometer * 104.8micrometer
Total Power dissipation	22.49microWatt
Static power dissipation	16.64microWatt
Dynamic power dissipation	5.85microWatt
FOM	4.6nJ
Absolute accuracy N_{abs}	9.96
Relative accuracy	6.02
Conversion rate	4Msample/sec
Offset error	0.999
Gain	73.2db

XII. CONCLUSION

8 bit pipelined ADC is designed in this paper with high gain, high speed and low power dissipation.

ACKNOWLEDGMENT

We would like to express our gratitude to KIIT university , Bhubaneswar, Odisha for providing CADENCE EDA Tool, used to carry out our work successfully in designing pipelined ADC. I wish to thank Mr. Rajendra Prasad for his guidance to complete our simulation work.

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BIOGRAPHIES

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Rajendra Prasad Currently he is an Assistant Professor(1) at KIIT University, Orissa since 2013.He has completed his M.TECH from VIT ,Vellore. He has published number of research papers in reputed journals and conferences. His research interest includes mixed-signal CMOS VLSI design, high-level synthesis and optimization of analog circuits. System at School of Electronics Engineering under KIIT University, Bhubaneswar, Odisha. His area of research includes analog and mixed signal IC design and optimization